WDR

1/3-Inch D1 WDR CMOS Image Sensor ZA03W10

Brief data sheet

Version 1.3

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Applications

- security and surveillance cameras
- automotive cameras

Features

- **Wide Dynamic Range(WDR)**
- **Automatic controls** :

automatic exposure control(AEC), automatic gain control (AGC), automatic black level calibration (ABLC), automatic white balance (AWB),
auto flicker detection (AFD)

- **Programmable controls** :

exposure, gain, frame rate, horizontal mirror, vertical flip, scaling, windowing

- **Image adjusting functions** :

lens shading correction, color correction, gamma correction, hue and saturation, brightness, contrast, sharpness(edge enhancement), false color suppression, chroma suppression

- Efficient denoising coupled with defective pixel correction
- Support for eclipse cancellation
- Support for flash strobe and output enable
- Support for serial interface compatible with I^2C
- Support for output formats :
  10-bit raw / denoised / ISP Bayer, YUV422, BT656, HREF, RGB565
- Support for image size :
  720×480p @ 60fps / 30fps
  VGA @ 60fps / 30fps
- Support for input clock : 13.5/18/27/54MHz
- On-chip phase locked loop (PLL, 108MHz)

Key specifications

- **Active pixel array** : 720H X 480V
- **Optical format** : 1/3 inch
- **Pixel size** : 6.9um X 6.9um
- **Scan mode** : progressive
- **Shutter** : rolling shutter
- **Maximum image transfer rate** :
  720×480p and VGA (Bayer) : 60fps
  720×480p and VGA (YUV) : 60fps
- **Output interface** : 10-bit parallel
- **Output formats** : 10-bit raw / denoised / ISP Bayer, YUV422, BT656, HREF, RGB565
- **Sensitivity** : 7.7V/Lux.sec
- **SNR** : 39.5dB
- **Dynamic range** : 90dB(@gain 8X)
- **Dark current** : 44.0mV/sec@60℃
- **Input clock frequency** : 13.5/18/27/54MHz
- **On-chip phase locked loop (PLL):** 108MHz
- **Power supply** :
  analog : 3.3V ± 10%
  core : 1.8V ± 5%
  I/O : 2.6~3.6V (3.3V Typical)
- **Power requirement** :
  active : 223mW
  standby : 611uW (master clock on)
  power down : 178uW (master clock off)

1. Signal Descriptions

Table 1-1 lists the signal descriptions and their corresponding pin names for the ZA03W10 image sensor. Refer to the “chip information” file for the package information.

Table 1-1 Signal Descriptions (sheet 1 of 2)

Name	I/O Type	Functions / Descriptions
ATEST	Output	Analog test pin.
AVDD	Supply	Analog power 3.3V with 0.1uF to AGND. †
AGND	Supply	Analog power ground.
PVDD	Supply	Pixel power 3.3V with 0.1uF to AGND. †
AGND	Supply	Analog power ground.
AVDD	Supply	Analog power 3.3V with 0.1uF to AGND. †
AGND	Supply	Analog power ground.
RVDD	Supply	Internal regulator power 3.3V with 0.1uF to AGND. †
IOVDD	Supply	I/O power 2.6V~3.3V with 0.1uF to IOGND. †
PLLGND	Supply	PLL power ground.
SYSCLK	Input	Master clock. (13.5/18/27/54 Mhz)
PLLVDD	Supply	PLL control block power 1.8V with 0.1uF to PLLGND. †
DGND	Supply	Digital power ground.
D9	I/O	Parallel pixel data output 9.
D8	I/O	Parallel pixel data output 8.
D7	I/O	Parallel pixel data output 7.
DVDD	Supply	Digital power 1.8V with 0.1uF to DGND. †
D6	I/O	Parallel pixel data output 6.
D5	I/O	Parallel pixel data output 5.
D4	I/O	Parallel pixel data output 4.
IOGND	Supply	I/O power ground.
D3	I/O	Parallel pixel data output 3.
D2	I/O	Parallel pixel data output 2.

†. The decoupled capacitors must be tied to the corresponding ground pins.

Table 1-1 Signal Descriptions (sheet 2 of 2)

Name	I/O Type	Functions / Descriptions
D1	I/O	Parallel pixel data output 1.
D0	I/O	Parallel pixel data output 0.
PIXCLK	Output	Pixel clock. Data can be latched by external devices at the rising or falling edge of PIXCLK. The polarity and drivability can be controlled.
DVDD	Supply	Digital power 1.8V with 0.1uF to DGND. †
DGND	Supply	Digital power ground.
HSYNC	I/O	Horizontal synchronization output. Asserted when pixel data output is valid.
VSYNC	I/O	Vertical sync : Indicates the start of a new frame.
IOVDD	Supply	I/O power 2.6V~3.3V with 0.1uF to IOGND. †
SDATA	I/O	Two-wire serial interface data.
SCLK	Input	Two-wire serial interface clock.
FSTROBE	Output	Flash or LED strobe output.
SADR1	Input	Two-wire serial interface slave address bit5.
SADR0	Input	Two-wire serial interface slave address bit2.
OUTEN	Input	Data output enable. When OUTEN is ‘LOW’, D[9:0] are tri-state mode. But, sensor is operation or not.
RSTB	Input	Asynchronous system reset. All registers are set to their default values.
STDBY	Input	Power down sensor operation. When STDBY=‘1’ there is neither current flow in any analog circuit branch, nor any beat of digital clock. D[9:0] and PIXCLK, HSYNC, VSYNC pins can be controlled to be all ‘1’ or all ‘0’ or tri-state. But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
TE	Input	Chip test mode enable.
IOGND	Supply	I/O power ground.
DVDD	Supply	Digital power 1.8V with 0.1uF to DGND. †
DGND	Supply	Digital power ground.